Digital Design Lab 7

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Section L001

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**Abstract**

The purpose of this lab was to create an up/down counter using Quartus II. The circuit was then tested using a simulation.

**Introduction**

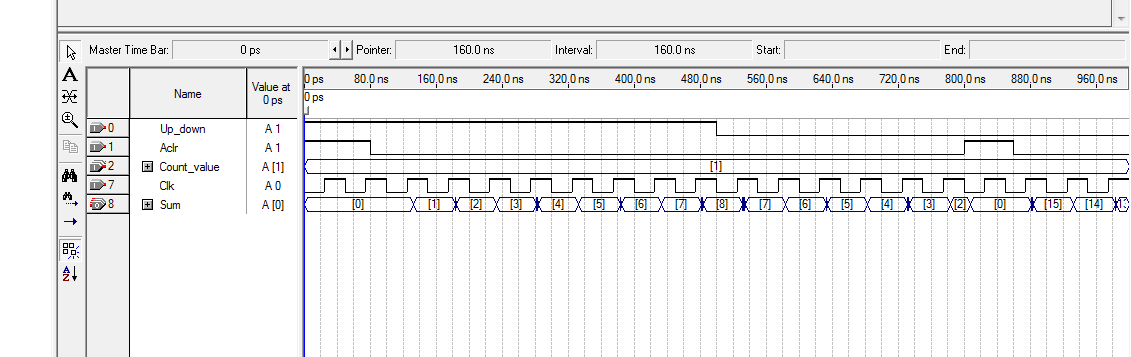
An up/down counter is a circuit made up of an adder/subtractor and a D flip-flop. It takes in an input up\_down, which decides whether the up/down counter counts up or down, an input bus Count\_value, which is four bits and determines what the counter counts up or down by (count\_value of 2 makes the counter output 2, 4, 6, 8, …), an input clk which updates output Sum when the clock's edge rises, and input Aclr which, when set to 1, makes Sum reset to all 0s. Inputs up\_down and Count\_value are fed into the adder/sub, and inputs clk and Aclr are fed into the D flip-flop. The D flip-flop outputs a 4-bit bus called Sum.

In this lab, the user created an up/down counter by using two different members of the LPM family: an adder/subtractor and a D flip-flop. The circuit was created and simulated in Quartus II. The circuit was tested using two values of Count\_value: 1 and 2. The circuit successfully counted up and down by 1, and it worked again when counting by 2.

**Design and Implementation**

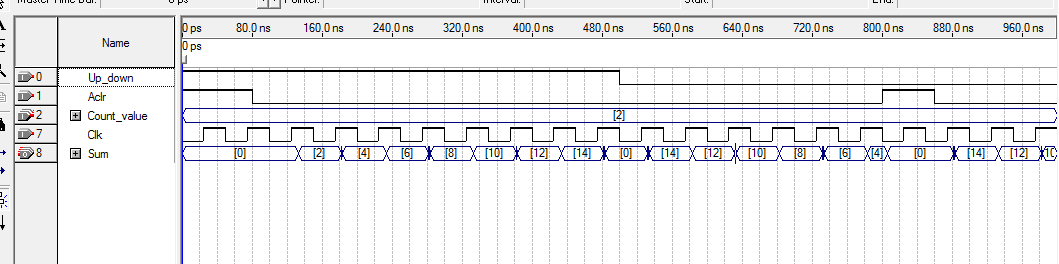
In order to create an up/down counter, a new Quartus project was created and a blank schematic diagram was added to it. A 4-bit adder/sub was added to the diagram, and a D flip-flop was put beside it. The four inputs were created: Count\_value[3..0] and up\_down for the adder/sub, and clk and Aclr for the D flip-flop. The output bus Sum[3..0] was created and wired as the output for the flip-flop. Once everything was completely connected, the project was compiled.

After the project compiled successfully, a waveform file was created to test the circuit. In the waveform file, the up\_down input was set as 1 for the first 500 ns and 0 for the rest of the time. Because of this, it was expected that the circuit would count up for the first 500 seconds and count down after that. Clk was set to be a periodic signal of 50 ns. Aclr was set to 1 from 0 to 80 ns and from 800 to 860 ns. For the first simulation, Count\_value was set as 1. The simulation was run, and the results of this simulation are shown in Figure 1 below.



**Figure 1**: up/down counter simulation results. In this simulation, Count\_value = 1.

The simulation was run once more, but this time Count\_value was set to 2. The simulation results are shown in Figure 2 below.



**Figure 2**: up/down counter simulation results. In this simulation, Count\_value = 2.

**Results**

The circuit correctly counted up and down by 1. It was also correct when counting by 2.

**Conclusion**

The lab was designed to give students a hands-on experience with creating and using an up/down counter. Using Quartus II, an up/down circuit was implemented and tested with simulations. The lab took about 30 minutes to complete.